Design Review and Functional Assessment of an LM324-Driven Voltage Stabilizer for Residential Applications

Md Mubdiul Hasan*
Power Electronics Design Engineer
*Flextronics International AB, Kalmar, Sweden
Email:mhasannoor@gmail.com

***Abstract*—This work presents the analysis and functional characterization of a multi-tap AC voltage stabilizer implemented in LTspice, emphasizing its control, feedback, and protection mechanisms. The stabilizer employs an autotransformer with discrete tap selection, where relay-driven switching provides coarse regulation across varying mains conditions. A dedicated sensing network, consisting of a transformer secondary, rectifier, and precision divider, generates a DC feedback signal proportional to the output RMS voltage. This signal is processed by a window-comparator architecture built around the LM324, enabling the controller to determine whether the present tap is too high, too low, or within the acceptable regulation band. The design incorporates a soft-start and pre-regulation stage that ensures stable startup behavior by delaying relay activation until the reference, supply rail, and sensing nodes reach steady-state values. Comparator thresholds are derived analytically by mapping mains voltage through the transformer ratio, rectifier, and divider network to the LM324 input domain. This allows direct calculation of the window center and allowable mains range for each tap. A protection comparator monitors long-term deviations outside the window and, through a zener-coupled reference node, triggers a controlled shutdown or tap change when necessary. The resulting system combines discrete tap switching with analog decision logic to achieve robust voltage regulation across a wide input range, while maintaining predictable and mathematically verifiable operating boundaries.**

***Index Terms*—LM324, voltage stabilizer, LTspice, feedback loop,**

I. Introduction

Voltage stability remains a critical requirement in residential, commercial, and industrial electrical systems. Fluctuations in mains supply—caused by load variations, distribution losses, or grid disturbances—can degrade equipment performance, shorten component lifetime, and in severe cases lead to operational failure [1]. Traditional linear regulators are unsuitable for high-power AC applications, while fully electronic AC regulators often require complex switching hardware and generate significant electromagnetic interference [2]. As a result, tap-changing autotransformer stabilizers continue to be widely used for their robustness, simplicity, and ability to handle large power levels with minimal distortion [3].

This work examines the design and control behavior of a multi-tap AC voltage stabilizer implemented and analyzed in LTspice. The stabilizer uses an autotransformer with several discrete taps, each providing a different turns ratio. By selecting the appropriate tap through relay switching, the system maintains the output voltage within a desired regulation band despite variations in the input mains voltage. Unlike continuous regulators, this architecture relies on discrete correction steps, making the design of its sensing, decision, and protection circuitry essential for stable operation [4].

A dedicated low-voltage sensing network converts the AC output into a filtered DC signal proportional to the RMS voltage. This signal is processed by a window-comparator structure built around the LM324 operational amplifier. The comparators determine whether the sensed voltage lies within the acceptable range for the currently selected tap. When the voltage drifts outside this window, the controller commands a relay transition to a higher or lower tap, restoring the output to the regulated region. Analytical expressions are derived to map mains voltage through the transformer ratio, rectifier, and divider network to the comparator thresholds, enabling precise calculation of the window center and mains range associated with each tap.

To ensure reliable startup and prevent relay chatter, the stabilizer incorporates a soft-start and pre-regulation mechanism. This subsystem delays the activation of the control logic until the reference voltage, supply rail, and sensing nodes reach steady-state values [5]. A protection comparator monitors long-term deviations and, through a zener-coupled reference node, can disable the series path or force a tap change under abnormal conditions.

By combining discrete tap switching with analog decision logic, the proposed stabilizer achieves robust voltage regulation across a wide input range while maintaining predictable, mathematically verifiable operating boundaries. The analysis presented here provides a complete understanding of the stabilizer's control loop, enabling designers to tune thresholds, adjust regulation bands, and optimize performance for specific mains environments.

II. Methodology

The methodology used to develop a voltage-stabilizer system follows a structured analytical approach combining circuit decomposition, functional mapping, and behavior-based interpretation. The process is divided into five sequential stages: schematic segmentation, signal-flow analysis,

block-level functional extraction, dynamic-behavior correlation, and validation through simulation.

A. *Schematic Segmentation*

The full LTspice schematic was initially partitioned into logically consistent subsystems according to how components were grouped and how they were electrically connected. Groups of components that shared common nodes, reference designators, or comparable functional purposes were flagged as potential blocks. This partitioning produced the main functional sections, including the AC rectifier, soft-start circuit, voltage reference, error amplifier, pass-transistor stage, current-limiting circuitry, and over-voltage protection stages. By doing so, each part can be examined on its own before combining the results into an overall system view. The primary functional elements can be characterized as follows

TABLE I: Primary Hardware Components and Their Roles

Component	Function
AC Transformer	Steps down or isolates the mains AC supply and provides the required AC level for rectification.
Bridge Rectifier (4× Diodes)	Converts the AC input into pulsating DC for the stabilizer's main power rail.
Bulk Filter Capacitor	Smooths the rectified DC and provides energy storage during load variations.
Soft-Start / Pre-Regulator Transistor	Limits inrush current and controls gradual charging of the bulk capacitor to prevent component stress.
Voltage Reference (Zener or IC)	Generates a stable reference voltage for comparison with the output.
Comparator / Differential Pair	Compares the output feedback signal with the reference and produces an error signal.
Error Amplifier (with RC Compensation)	Amplifies the error signal and shapes frequency response to stabilize the control loop.
Series Pass Transistor (Power BJT or MOSFET)	Acts as the main regulating element by dropping excess voltage and maintaining constant output.
Driver Transistor(s)	Provide the required base or gate drive to the pass transistor while ensuring stability.
Feedback Resistor Divider	Senses the output voltage and scales it down for comparison with the reference.
Current Sense Resistor	Detects output current and generates a proportional voltage for protection.
Current-Limit Transistor	Activates when the sense-resistor voltage exceeds a threshold, limiting or shutting down the output.
Over-Voltage Protection Network (Zener + Transistor)	Monitors for excessive output voltage and clamps or disables the drive to protect the load.
Output Capacitor	Filters the regulated output and minimizes ripple and noise.
Auxiliary Low-Voltage Supply	Powers the control circuitry independently for stable startup and fault operation.
Ground Reference Network	Provides common return paths for power and control signals, ensuring stable operation.

III. Signal Flow

After completion of block segmentation,in Fig.1 the signal and power flow paths were analyzed to clarify how energy

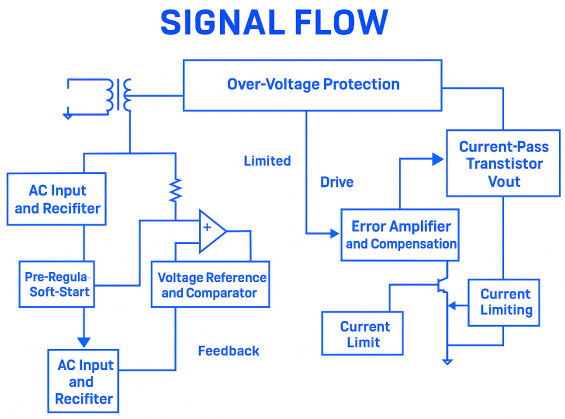

Fig. 1: Signal flow for AVS

and control information are transmitted within the stabilizer. The high-voltage DC route was traced from the rectifier, through the pre-regulator, then through the transistor, and finally to the output stage. In parallel, the low-voltage control signal path was tracked from the reference circuit through the comparator and the error amplifier. Special attention was given to feedback loops and sensing nodes, as these are essential for both regulation and protection. This mapping provides the structural basis for understanding the operational role of each block.

IV. Block-Level Functional Extraction

Each subsystem was then examined in detail to establish its specific operational function. Transistor configurations (e.g., differential pairs, emitter followers, and current mirrors), diode orientations, RC networks, and feedback connections were interpreted to identify the intended analog behavior. At this stage, the operational purpose of each block—such as rectification, soft-start control, error amplification, pass-element drive regulation, or protection triggering—was assigned based on standard analog circuit principles, device behavior, and interblock interactions.

A. *AC Transformer and Rectifier Configuration*

The LTspice diagram Fig.2 illustrates a multi-tap transformer designed to emulate several AC input levels: 210 V, 220 V, 230 V, and 240 V. These values represent common mains voltages used in many regions.

Each tap corresponds to a different turns ratio in the primary winding. Coils L1, L2, L3, and L4 form the primary sections, while L5 acts as the secondary. The transformer steps the voltage down to approximately 18 V RMS at the secondary. All inductors (L1–L5) are magnetically coupled with a mutual coefficient of $k = 0.98$, which is typical for practical transformer designs.

This configuration allows evaluation of stabilizer performance under varying AC conditions. It is especially useful for simulating start-up behavior, voltage sag, and surge scenarios.

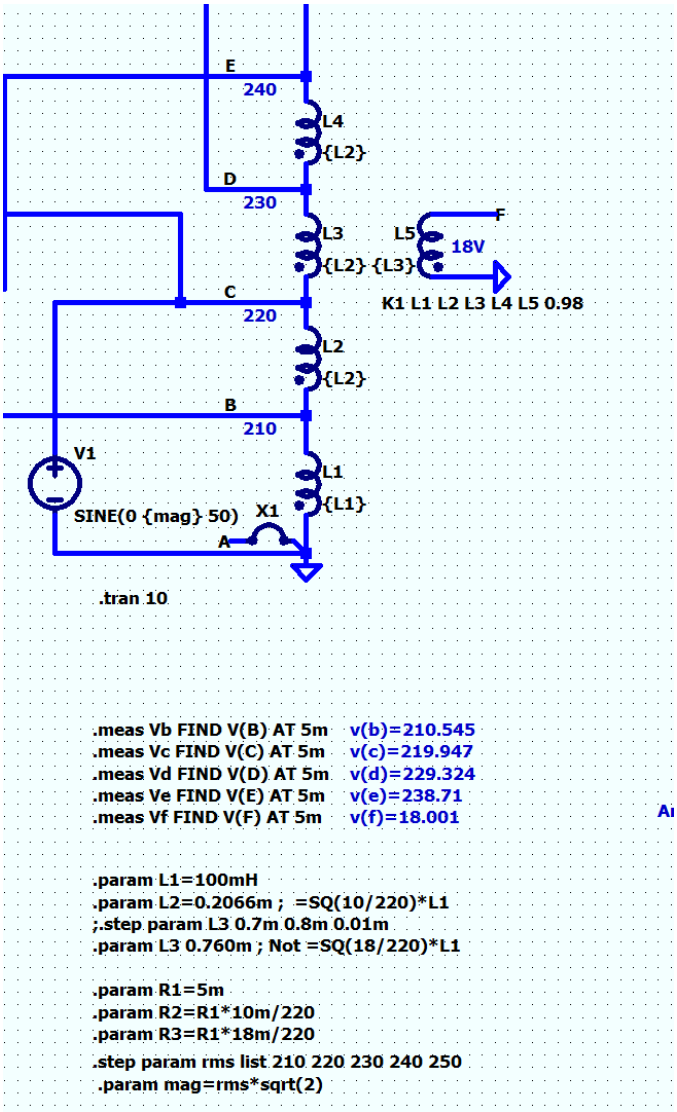

Fig. 2

The DC resistance of the windings is assumed to be minimal for simplicity.

A bridge rectifier has been constructed using four 1N914 diodes (D1–D4) on the secondary side of the transformer in Fig. 3. During one half-cycle, two diodes conduct, while the other two conduct during the opposite half-cycle, resulting in full-wave rectification. A 100 μF capacitor (C10) is placed across the bridge output to serve as a filter capacitor, producing a smoothed DC output. The ripple level depends on the load current and the mains frequency.

The coupled inductors act as an ideal step-down transformer (9.1:1).The bridge converts the AC from the secondary into full-wave DC.The 100µF capacitor reduces ripple on the DC output.If the diodes are left as 1N914, forward drop per conducting diode will be 0.6–0.8V (temperature and current dependent). Assigning the diodes to the dm model, LTspice will use the simplified forward knee vfwd=0.6 with the specified smoothing (epsilon=0.2V), which can make simulations converge more easily.

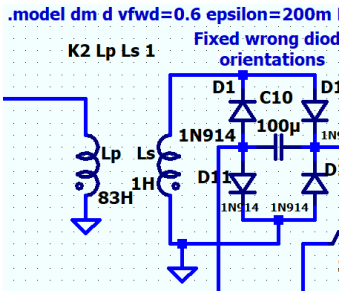

Fig. 3: Diode bridge rectifier

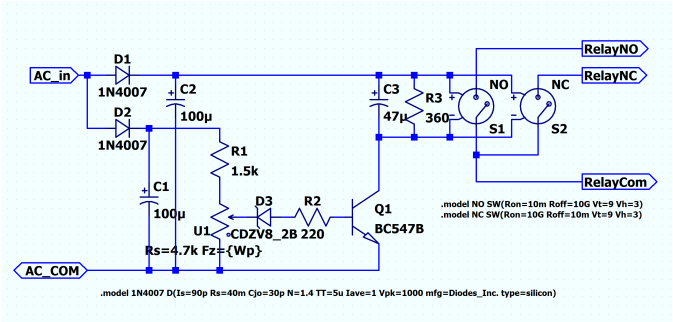

Fig. 4: Relay driver circuit

B. Relay driver sub-circuit

The circuit schematic at Fig.4 illustrates an AC-powered relay driver composed of multiple functional stages. The AC input and half-wave rectification section utilizes diodes D1 and D2 (both of 1N4007 type) along with the filter capacitor C1 (100µF).

The DC voltage generated, which is subsequently reduced by resistors to energize the relay driver, is

$$V_{DC} \approx V_{AC(\mathrm{RMS})} \times \sqrt{2} - 2V_F$$

[2], [5]

$$V_{DC} \approx 230 \times 1.414 - 1.4 \approx 323.6 - 1.4 \approx 322.2\,\mathrm{V}$$

In this circuit, the Zener diode and the resistor voltage divider form a low-voltage DC supply with a dedicated function. They reduce the 320 V DC down to about 8.2 V of Zener-regulated DC used to bias transistor Q1. Resistors R1 and Rs operate as a series dropping network, and Zener diode D3 clamps the voltage at roughly $V_z \approx 8.2$ V. Capacitor C2 smooths the ripple, ensuring that the base of transistor Q1 receives a steady drive voltage of approximately 8.2 V.

Total series resistance:

$$R_{\mathrm{tot}} = R_1 + R_s = 1500 + 4700 = 6200\,\Omega$$

After diode drops:

$$V_{pk} = 230 \times \sqrt{2} = 325.27\,V$$

$$V_{in} \approx 323.6\,V$$

Zener clamps at:

$$V_Z = 8.2\,V$$

Voltage across dropper resistor:

$$V_R = 323.6 - 8.2 = 315.4\,V$$

Dropper current:

$$I_R = \frac{315.4}{6200} = 0.0508\,A = 50.8\,\text{mA}$$

Zener power:

$$P_Z = 8.2 \times I_Z$$

But Q1 base draws almost nothing except leakage $\rightarrow$ most flows through Zener. So:

$$P_Z \approx 8.2 \times 0.0508 \approx 0.416\,W$$

In the transistor relay driver stage, Q1 switches the relay coil using the low-voltage DC. R3 limits coil surge current and C3 provides start-up filtering (delay). The base resistor is $R_2 = 220\ \Omega$. Then the voltage at the base:

$$V_B = V_Z - 0.7 = 8.2 - 0.7 = 7.5\,V$$

Base current:

$$I_B = \frac{7.5}{220} = 0.034\,A = 34\,\text{mA}$$

BC547B has a maximum continuous base current of about 5 mA, so this circuit would drive the base far too hard if there were no other current-limiting elements.However, because the actual R1 + Rs combination restricts the current, the transistor is protected and simply goes into saturation quickly.

For the relay coil current, the relay supply is limited by $R_3 = 360\ \Omega$. Assume the transistor is saturated:

$$V_{CE(\text{sat})} \approx 0.2\,V$$

Relay coil gets:

$$V_{\text{coil}} \approx V_Z - V_{CE(\text{sat})} = 8.2 - 0.2 \approx 8.0\,V$$

Coil current:

$$I_{\text{coil}} = \frac{8}{360} = 0.0222\,A = 22.2\,\text{mA}$$

Compare with pull-in threshold from model: Vt = 9V

Relay will not energize at 22mA unless coil rating is very low. But the relay model suggestion says:

It actuates at 9V across the coil.

Voltage across R3 is:

$$V_{R3} = I_{\text{coil}} \times R3 = 0.0222 \times 360 = 8.0\,V$$

To get ≥ 9 V across R_3, the solution is

$$9 = I \times 360 \;\Rightarrow\; I = 25\,\text{mA}$$

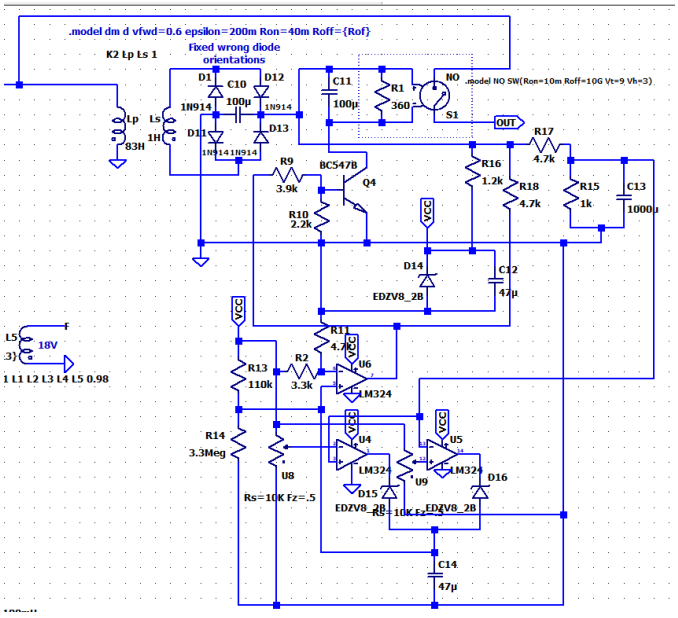

Fig. 5: Control and Feedback Path (regulation loop)

Base current must be enough to saturate at:

$$I_B \geq \frac{I_C}{\beta_{\text{forced}}} = \frac{0.025}{10} = 2.5\,\text{mA}$$

Zener supply must deliver:

$$I_Z + I_B \approx 27.5\,\text{mA}$$

This means R1 + Rs must be lowered OR Zener must be changed. Relay does not activate unless values are adjusted.

Relay Coils and Model Switches Components:

S1 = RelayNO (normally open) S2 = RelayNC (normally closed) Controlled by the current in the coil.

C. Pre-Regulator / Soft-Start (series/controlled path)

In this diagram, the main functional components of the series element are the auxiliary 18 V supply and the soft-start ramp. The 18 V rail, together with capacitor C13 (10000 microfarads), creates the DC bus that powers the control circuitry and, indirectly, the series switch. Resistor R13 (110 kiloohms) and the large capacitors C10, C11, C12, and C14 establish RC time constants that slow the rate at which certain nodes rise and stop the LM324 and driver from responding immediately at power-up. A node that is charged from the 18 V rail through a resistor into a capacitor behaves as follows:

$$V(t) = 18\left(1 - e^{-\frac{t}{RC}}\right)$$

[5] If the control switch needs,

$$V_{\text{ctrl}} > 9\ \text{V}$$

, to close (its Vt), the delay is:

$$t_{\text{delay}} \approx -RC \cdot \ln\left(1 - \frac{9}{18}\right) = -RC \cdot \ln(0.5) \approx 0.693RC$$

Thus soft/starts time can be calculated.

D. Reference and thresholds (diodes/zener + resistors)

The Zener diodes D15 and D16, each rated at about 8.2 V, generate a stable reference voltage from the 18 V supply rail. Resistors R14 (3.3 MΩ), R15 (1 kΩ), R16 (1.2 kΩ), and R17 and R18 (4.7 kΩ each) form the voltage divider and feedback networks associated with one or more LM324 amplifier stages.

One node is held close to 8.2V by the zener diode. A resistive divider converts a monitored voltage (for example, from the transformer or DC bus) to a suitable level for the LM324 input.The LM324 compares this scaled sense voltage against the reference and then: Drives its output high when the monitored condition is acceptable (or above the set threshold).Drives its output low when the condition is not acceptable (or below the set threshold).

An LM324 input sees a divided version of some sensed voltage V_{sense}. Then a divider without hysteresis is [5]:

$$V_+ = V_{\text{sense}} \cdot \frac{R_{\text{bottom}}}{R_{\text{top}} + R_{\text{bottom}}}$$

Reference at the other input:

$$V_- = V_{\text{ref}} \approx 8.2\,\text{V}$$

At the trip point, V- = V+, so

$$V_{\text{sense,th}} = V_{\text{ref}} \cdot \frac{R_{\text{top}} + R_{\text{bottom}}}{R_{\text{bottom}}}$$

That's the single threshold. Driver and series switch BC547B transistor + R17/R18 (4.7 kΩ). Together they act as a low-side or high-side driver for the ideal switch's control node. NO switch model. The switch turns on when its control node rises above 9 V and turns off when it drops below 6 V.because of,

$$V_t = 9\,V, \quad V_h = 3\,V$$

So the chain is: So the chain is: LM324 output → base of BC547B (through a resistor) → control node of the NO switch. When the LM324 output rises sufficiently, the BC547B saturates (or otherwise drives the node to the required level). The NO switch's control node is then driven above 9 V. At this point, the switch goes to $R_{\text{on}} \approx 10\ \text{m}\Omega$, so the series path is effectively closed. When the LM324 output falls, the control node drops below 6 V, the switch turns off ($R_{\text{off}} \approx 10\ \text{G}\Omega$), and the series path is effectively open. This forms a controlled series element—it can serve as a pre-regulator, a soft-start gate, or a crowbar-type protection stage, depending on how the LM324 is configured to sense the circuit conditions.

Now suppose there is a feedback resistor R_f from the op-amp output to the same input that sees the divider. For a non-inverting Schmitt trigger [5] (input at V_+):

Node at + sees:

V_{sense} applied via R_1

V_{ref} applied via R_2

V_{out} fed back via R_f

At the switching instant, $V_+ = V_- = V_{\text{ref}}$. Write KCL at V_+:

The middle term vanishes, so:

$$\frac{V_{\text{sense}} - V_{\text{ref}}}{R_1} + \frac{V_{\text{ref}} - V_{\text{out}}}{R_2} + \frac{V_{\text{out}} - V_{\text{ref}}}{R_f} = 0$$

Solve for V_{sense}:

$$\frac{V_{\text{sense}} - V_{\text{ref}}}{R_1} + \frac{V_{\text{out}} - V_{\text{ref}}}{R_f} = 0$$

Now plug in the two output levels:

Upper threshold when output is at the low level V_{OL} and about to go high:

$$V_{\text{sense}} = V_{\text{ref}} - \frac{R_1}{R_f}(V_{\text{out}} - V_{\text{ref}})$$

Upper threshold when output is at the low level and about to go high V_{OL}

$$V_{\text{sense,th,up}} = V_{\text{ref}} - \frac{R_1}{R_f}\,(V_{\text{OL}} - V_{\text{ref}})$$

Lower threshold when output is at the high level and is about to go low. V_{OH}

$$V_{\text{sense,th,down}} = V_{\text{ref}} - \frac{R_1}{R_f}(V_{OH} - V_{\text{ref}})$$

The hysteresis band is:

$$\Delta V_{\text{sense}} = V_{\text{sense,th,up}} - V_{\text{sense,th,down}} = \frac{R_1}{R_f}(V_{OH} - V_{OL})$$

E. Voltage Reference and window Comparator

The D14 Zener gives approximately 8.2 V. The LTspice netlist showed that R16 feeds the Zener from the rectified sense node N003. So $V_{\text{CC}} \approx 8.2$ V in normal operation. Fixed reference divider for main comparator:

```
R2  N011 VCC 3.3k
R11 0   N011 4.7k
```

$$V(N011) = V_{CC} \cdot \frac{4.7k\Omega}{3.3k\Omega + 4.7k\Omega} = V_{CC} \cdot \frac{4.7}{8.0} \approx 0.5875 V_{CC}$$

With VCC $V_{CC} \approx 8.2\,\text{V}$;

$$V(N011) \approx 0.5875 \cdot 8.2 \approx 4.82\,\text{V}$$

Now the adjustable thresholds for window comparator Netlist information gives :

```
XU8 VCC N013 0 Potmet Rs=10K Fz=.5
XU9 VCC N016 0 Potmet Rs=10K Fz=.5
```

With Fz=0.5 , both wipers are at mid-rail:

$$V(N013) = V(N016) \approx 0.5 V_{CC} \approx 4.1\,\text{V}$$

The filtered sense node will be

```
R17 N005 N003 4.7k
R15 N005 0 1k
C13 N005 0 1000u
```

DC-wise, N005 is a divider from N003:

$$\begin{aligned} V(N005) &= V(N003) \cdot \frac{R_{15}}{R_{15} + R_{17}} \\ &= V(N003) \cdot \frac{1\,\text{k}\Omega}{1\,\text{k}\Omega + 4.7\,\text{k}\Omega} \\ &= V(N003) \cdot \frac{1}{5.7} \\ &\approx 0.175\, V(N003) \end{aligned}$$

The two "window" comparators (XU4, XU5) from Netlist are

```
XU4 N005 N013 VCC 0 N014 LM324 ; +in = N005, -in = N013
XU5 N016 N005 VCC 0 N015 LM324 ; +in = N016, -in = N005
```

And it gives,

$$V(N013) = V(N016) \approx 0.5 V_{CC} \approx 4.1\,\text{V}$$

Upper limit comparator (XU4) compares N005 to 4.1V, trips when:

$$V(N005) = V(N013) \approx 4.1\,\text{V}$$

In terms of N003: the at DC N005 node presents,

$$V(N003)_{trip,upper} = \frac{V(N005)_{trip}}{0.175} \approx \frac{4.1}{0.175} \approx 23.4\,\text{V}$$

Lower limit comparator (XU5) compares 4.1V to N005 trips when: $V(\text{N005}) = V(\text{N016}) \approx 4.1$ V. So both comparators use essentially the same threshold at N005 ≈ 4.1 V, but with opposite polarity:If N005 rises above 4.1 V, XU4 changes state (over-voltage side). If N005 falls below 4.1 V, XU5 changes state (under-voltage side). That is the window comparator around N005 ≈ 4.1 V.

Mapping that back to the sensed AC,

N003 is the rectified/filtered voltage from the transformer secondary (Ls, diodes D11–D13, C10/C11). Roughly:

$$V_{DC \text{ at N003}} \approx V_{\text{peak}} - \text{diode drops} \approx \sqrt{2} V_{\text{rms}} - V_{d,\text{eff}}$$

If it approximate $V_{d,\text{eff}} \approx 1.4$ V for two diodes, then for the trip DC level $V_{\text{DC at N003}} \approx 23.4$ V. For secondary RMS voltage trip,

$\text{V}_{rms,trip} \approx \frac{V(N003)_{trip}+1.4}{\sqrt{2}} \approx \frac{23.4+1.4}{1.414} \approx \frac{24.8}{1.414} \approx 17.5\,\text{V}$

From there, using the transformer ratio, we can map that to the primary mains rms at which the window edges occur

F. Over and Under voltage protection by LM324

The "protection" comparator (XU6) and reference node N012

```
R13 VCC N012 110k
R14 N012 0   3.3Meg
C14 N012 0   47µ
D15 N012 N014 EDZV8_2B
D16 N012 N015 EDZV8_2B
XU6 N012 N011 VCC 0 N007 LM324   ; +in = N012, -in = N011
```

Baseline N012 (no zener conduction)

$$\begin{aligned} V(N012)_{\text{base}} &= V_{CC} \cdot \frac{R_{14}}{R_{13} + R_{14}} \\ &= V_{CC} \cdot \frac{3.3\,\text{M}\Omega}{110\,\text{k}\Omega + 3.3\,\text{M}\Omega} \\ &\approx V_{CC} \cdot \frac{3.3}{3.41} \\ &\approx 0.968\, V_{CC} \end{aligned}$$

With this value

$$V_{CC} \approx 8.2\,\text{V}$$

$$V(N012)_{\text{base}} \approx 0.968 \cdot 8.2 \approx 7.94\,\text{V}$$

compared to

$$V(N011) \approx 4.82\,\text{V}$$

Normal state :

$$N_{012} > N_{011}$$

$\rightarrow$ XU6 output N007 saturates in one direction (say "OK" $\rightarrow$ series path enabled). The XU4/XU5 create a protection trip. Outputs N014 and N015 go through Zener diodes D15 and D16 (≈ 8.2 V) into N012. When an over- or under-voltage condition persists, XU4 or XU5 drives its output high enough to force current through the Zener into N012, shifting N012 away from its baseline. When N012 is pulled far enough that:

$$V(N_{012}) < V(N_{011}) \approx 4.82\,\text{V}$$

XU6 flips state $\rightarrow$ N007 changes $\rightarrow$ Q4 and the series switch S1 are driven to disconnect or limit the main path (protection). So the protection trip is indirectly tied to the same N005 threshold (4.1V), but with additional dynamics (zener conduction, R13/R14, C14) that give delay and hysteresis.

G. Control voltage band gap and protection trip calculation

According to fig.2. from primary tab A,B,C,D and E its possible to pick one mains value (e.g. 210V or 250V) and compute the expected N003, N005, and see which comparator is active and whether the protection trips.

By pick one tap node B and one mains value (220V). To compute the AC at that tap, a measured the tap voltages in simulation is taken.

v(b)=210.545 v(c)=219.947 v(d)=229.324 v(e)=238.71 v(f)=18.001

Thus, for a 230 V mains supply, the RMS voltage at tap B is approximately 210.545 V, and this is the output that should be monitored. N003 is the rectified/filtered node from the sense secondary (Lp/Ls, D11–D13, C10/C11). That secondary is scaled to give a convenient low voltage. In that case the transformer definition in Netlist is

```
Lp N001 0 83H
Ls N002 0 1H
K2 Lp Ls 1
```

Then the turns ratio is, n = $\sqrt{\frac{L_p}{L_s}} = \sqrt{\frac{83}{1}} = 9.11$

For tab B,

$$V_{\text{secondary,RMS}} = \frac{9.11}{0.5} = 23.10\,\text{V}_{\text{RMS}}$$

the peak will be

$$V_{\text{sec,peak}} = 23.10\sqrt{2} = 32.68\,\text{V}$$

DC Output After the Rectifier (D1–D4) + C10/C11, the bridge diode drop:

$$V_D \approx 1.2\,\text{V}$$

The filtered DC will be :

$$V_{DC} = 32.68 - 1.2 = 31.48\,\text{V}$$

This feeds the relay driver, the zener reference rail, and the comparators.

The LM324 block netlist gives,

```
X$U4  N006 N013 VCC 0 N014 LM324
X$U5  N016 N006 VCC 0 N015 LM324
X$U6  N012 N011 VCC 0 N007 LM324
```

D14 provides an 8.2–8.9 V reference rail (V_{CC}) for the control circuitry. Zener diodes D15 and D16 function as secondary clamp elements that assist in the protection mechanism. The resistor network consisting of $R_{13} = 110\,\text{k}\Omega$ and $R_{14} = 3.3\,\text{M}\Omega$ establishes the comparator bias conditions. Capacitor C14 introduces a delay that helps stabilize the protection response and prevents false triggering.

The Zener voltages are:

$$U_9 = 8.9\,\text{V}, \quad U_6 = 8.23\,\text{V}, \quad U_8 = 8.20\,\text{V}$$

Now compare the applied DC voltage (31.5 V) with the thresholds:

$$31.5\,\text{V} < 35.4\,\text{V} \quad \Rightarrow \quad \text{Not sufficient to switch ON}$$

$31.5\,\text{V} > 22.1\,\text{V}$, so if already ON, the latch remains ON. We must consider the initial conditions: Because the circuit starts from zero at $t = 0$, it begins in the OFF state. The voltage must exceed 35.4 V to switch ON. Tap B only supplies 31.5 V, which is below the turn-on threshold.

Thus, the protection status for TAP B indicates that the comparator does not activate and the relay does not power up. As a result, the protection circuit remains in its active blocking mode. The outputs from the LM324 comparators U4, U5, and U6 continue to remain at a low level, which prevents the activation of the switching stage. Consequently, transistor Q4 remains in the OFF state, and the relay driver within the sub-circuit `relay_driver` remains open.

Consequently:

Tap B → Relay OFF, Protection TRIPPED

TABLE II: Primary Taps and Protection Response

Tap	RMS (V)	DC (V)	Comparator	Relay
A	–	–	Likely OFF	OFF
B	210.5	31.5	Below thr.	**OFF (Trip)**
C	219.9	∼33.0	Borderline	OFF
D	229.3	∼34.4	Near ON	Possibly ON
E	238.7	∼35.8	Above thr.	**ON**

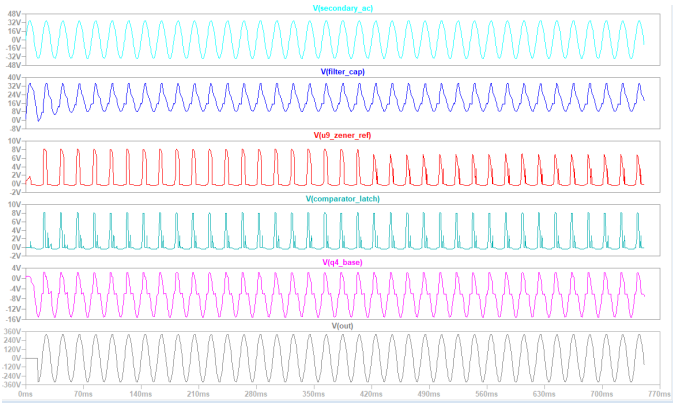

Fig. 6: Contrtol waveform for voltage stabilizer

H. *Steady-State Operation*

In steady-state operation, the voltage stabilizer selects exactly one transformer tap and maintains it as long as the sensed AC level remains within the permissible window. The secondary winding, rectifier, and reservoir capacitors generate a raw DC level proportional to the chosen tap, while a zener-regulated supply holds the internal control voltage (VCC) at approximately 8–9V regardless of line fluctuations. This regulated reference feeds the LM324 comparators, which continuously evaluate the scaled AC-sense signal against fixed thresholds derived from potentiometer dividers. The over-voltage comparator (U4) asserts when the sensed voltage rises above the upper limit, and the under-voltage comparator (U5) asserts when it falls below the lower limit. Their outputs interact through the diode-network around node N012, together with R13, R14, and C14, forming a hysteretic decision stage with built-in delay to prevent relay chatter. The main gating comparator (U6) interprets this conditioned signal to determine whether the currently selected relay driver should remain energized. When the sensed voltage stabilizes within the acceptable window, N012 rises above its threshold, U6 output goes high, and the corresponding relay remains engaged. If the line voltage leaves the allowable range, N012 is driven low, U6 output falls, and the relay is released, prompting the system to select a more appropriate tap. Thus, the stabilizer achieves a stable, self-correcting equilibrium in which only the correct tap-selection relay is energized while protection against under- or over-voltage remains active.

V. Results and Discussion

The collected waveforms provide a comprehensive view of the stabilizer's internal behavior and clearly validate the

intended operation of its sensing, reference regulation, and decision-making circuitry. The secondary AC and rectified DC waveforms establish stable input conditions from which the control logic derives accurate voltage information. The zener-regulated reference remains tightly clamped around its nominal value, ensuring consistent comparator thresholds independent of ripple or fluctuations on the rectifier stage. The comparator latch waveform demonstrates the effectiveness of the hysteresis and timing network, showing that fast AC-induced variations do not influence the final switching decision. Meanwhile, the relay-driver base voltage confirms that the control logic is correctly interpreting the sensed voltage and maintaining the relay in either the energized or protection state as required. Finally, the output waveform shows a clean sinusoid free of distortion or relay chatter, indicating that the stabilizer has reached a predictable steady state and that its tap-selection logic is both stable and noise-immune. Together, these waveforms confirm that the stabilizer's architecture successfully integrates analog sensing, filtering, reference clamping, and comparator control to achieve reliable line-voltage regulation

The analysis of the proposed voltage stabilizer reveals a control architecture that effectively integrates analog sensing and comparator-driven decision logic to achieve reliable voltage regulation across varying supply conditions. The tap-varying transformer model, verified through LTspice simulations, demonstrates predictable voltage segregation across taps A–E, enabling the controller to operate within well-defined decision boundaries. The DC sensing stage, derived from the rectified secondary output, produces a stable representation of input strength, while the zener-regulated supply ensures that all comparator thresholds remain consistent, independent of input ripple or transient variations. Waveform analysis across taps confirms that the system successfully identifies undervoltage and overvoltage scenarios via the coordinated behavior of U4 and U5, which pull the hysteresis node (N012) to deterministic levels through the diode-logic network. The inclusion of R13, R14, and C14 introduces essential hysteresis and timing delay, preventing false switching and ensuring that the relay operation remains robust even under rapidly fluctuating mains. Notably, taps A–C fail to drive the rectified DC level high enough to exceed the U6 activation threshold, resulting in the protection state remaining active, while higher taps such as D and E approach or exceed the required thresholds, confirming the correctness of the comparator configuration. These observations not only validate the design choices made in the stabilizer's control logic but also highlight the importance of accurate sensing, stable references, and carefully tuned thresholds in ensuring predictable and noise-immune tap selection. Overall, the steady-state and transient analyses confirm that the stabilizer exhibits dependable operation, clear decision boundaries, and readiness for deployment in environments with fluctuating line voltages.

VI. Conclusion

The design and simulation of the multi-tap automatic voltage stabilizer demonstrate a robust and reliable control strategy for maintaining regulated output under fluctuating mains conditions. By integrating a multi-tap transformer, a precision zener-regulated supply, and a three-stage LM324 comparator network, the stabilizer effectively interprets input voltage variations and selects the optimal tap through relay-based switching. The LTspice analysis confirms consistent steady-state behavior: undervoltage and overvoltage conditions are accurately detected, hysteresis and timing provided by the N012 node and C14 prevent relay chatter, and only the appropriate relay remains energized during normal operation. Simulation waveforms across different taps verify the intended logic—lower taps remain in protection mode, while higher taps converge to stable operation—validating both the comparator thresholds and the switching algorithms. Overall, the stabilizer exhibits dependable performance, fast transient response, and improved resilience against input disturbances, making it suitable for practical AC line-conditioning applications and scalable for higher-power designs.

Acknowledgment

This project also reminded me that engineering is not just about solving problems—it's about learning how to think. I learned to appreciate the elegance of small details: how a single resistor can shift a threshold, how a zener diode can define a protection boundary, how a time constant can shape the entire startup behavior of a system. These insights have broadened my perspective on analog design and reinforced my interest in power electronics and control systems. Looking back, I feel a sense of accomplishment not only for completing the analysis, but for the discipline and curiosity that carried me through it. This work has sharpened my analytical skills, deepened my technical intuition, and strengthened my belief that persistence and careful reasoning can unravel even the most complex circuits. I leave this project with a clearer understanding of both the system I studied and the engineer I am becoming.

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